UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,716	04/23/2001	Jeffry J. Sniegowski	50060-00040	4806

7590 06/26/2003

MARSH FISCHMANN & BREYFOGLE LLP
3151 SOUTH VAUGHN WAY, #411
AURORA, CO 80014

EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	5

DATE MAILED: 06/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,716	SNIEGOWSKI ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,22-41,48-59 and 63-66* is/are rejected.

7)☒ Claim(s) *21, 42-47, 60-62* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3,4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-15,17-20, 22-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Barron et al (US 5,919,548)

Barron discloses a method for CMP of recessed microelectromechanical devices. This method comprises the steps of:

forming a first sacrificial layer 40 over a first substrate 10, (col 10, lines 6-7, fig. 31 of Barron shows that layer 40 has a lateral dimension that is generally parallel with an upper surface of substrate 10

forming a plurality of hollow etch channels 52 that extend laterally in the layer 40/first sacrificial layer (col 11, lines 15-17, fig. 4c), which reads on forming a plurality of discrete and at least generally laterally extending hollow conduits that are defined at least in part by first sacrificial layer

forming a layer 44 (polysilicon) over layer 40/first sacrificial layer (col 10, lines 48-49; fig. 3o), which reads on forming a first structural layer over the first sacrificial layer

removing sacrificial layer 40/first sacrificial layer by flowing wet etchant within the etch channels 52/plurality of conduits (col 11, lines 14-35)

Regarding claim 2, Barron discloses the step of forming the sacrificial layer using CVD.

Regarding claims 3, 4, Barron discloses the steps of forming a layer 42/first intermediate layer on layer 40/first sacrificial layer before forming layer 44/first structural layer, layer 42 is disposed between the layer 44 and layer 40 (fig. 3o), patterning layer 42 into a first assembly (fig. 3o), etching at least a portion of layer 40/first sacrificial layer to form undercut beneath the assembly (col 11, lines 12-13, fig. 4 c), forming a second sacrificial layer 24on the first sacrificial layer 40 (col 5, lines 14-15, fig. 3l)

Regarding claim 5, fig. 4c of Barron shows that first assembly remains after the step of removing sacrificial layer 40.

Regarding claim 6, fig. 3F of Barron shows that second sacrificial layer 24 is formed on the entirety of subassembly 16.

Regarding claims 7, 8, 9, 11, Barron discloses performing a planarizing step of the sacrificial layer using CMP (col 5, lines 15-17), etching through layer 24/ the second sacrificial layer to form openings 32/apertures, the opening allows for electrical interconnection (col 9, lines 24-29)

Regarding claims 10, 18, fig. 3r shows that assembly 42comprises a plurality of laterally extending strips.

Regarding claim 12, Barron discloses forming depression on an upper surface of layer 44/first structural layer and planarizing the upper surface of layer 44 (fig. 3o). Regarding claims 13, 19, fig. 3o of Barron shows that layer 44/first structural layer is formed after second sacrificial layer 24 is formed, layer 24 interconnects layer 44 and subassembly

42. Regarding claim 14, Barron discloses that layer 44/first structural layer is polysilicon (col 10, lines 48-50). Regarding claim 15, Barron discloses the step of etching/removing layer 42/subassembly (col 10, lines 51-52). Regarding claim 17, Barron discloses that layer 42/subassembly consisting of SiN (col 10, lines 35-36). Regarding claim 20, Barron discloses removing the second sacrificial layer 24 (col 8, lines 33-34). Regarding claim 22, fig. 3o of Barron shows that the openings/conduits are formed in the layer 40 before forming layer 44. Regarding claim 23, Barron discloses forming intermediate layer 36 (polysilicon) between layer 40 and the substrate (col 9, lines 32-33). Regarding claim 24, Barron discloses forming layer 44/first structural layer that does not have any openings/aperture (col 12, lines 35-37). Regarding claim 25, fig. 4b of Barron shows that layer 44 is movable after the step of removing the sacrificial layer 40. Regarding claims 26-35, fig. 4c of Barron shows that the etch channels 52/plurality of laterally extending hollow conduits are formed in parallel relation and equal spaced relation, the channels 52 also are radially extending in relation to a common center. Regarding claim 36, Barron discloses using a etchant that is not selective to layer 40 (col 11, lines 24-26). Regarding claim 37, Barron discloses encasing etch channels/hollow conduits with etch release rails 48 (fig. 4b). Regarding claim 38, Barron discloses forming runner 54 that is laterally spaced from the layer 44/first structural layer, layer 54/runner also interconnects with rails 48 (fig. 4c).

3. Claims 39-41, 48-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Barron et al (US 5,919,548)

Barron discloses a method for CMP of recessed microelectromechanical devices. This method comprises the steps of:

forming a first sacrificial layer 40 over a first substrate 10, (col 10, lines 6-7, fig. 31)

forming a layer 42/intermediate layer on the layer 40/first sacrificial layer (fig. 3p)

forming layers 48 and 50 from layer 42 that are disposed on and extend laterally to layer 40 (col 11, lines 1-5, fig. 3q), which reads on forming a plurality of first strips from the first intermediate layer that are disposed on and extend at least generally relative to the first sacrificial layer.

forming a second sacrificial layer 24 on first sacrificial layer 40 and alongside the plurality of layers 48, 50/strips (col 9, lines 7-8, fig. 3q)

forming a layer 44 (polysilicon) over layer 40/first sacrificial layer (col 10, lines 48-49; fig. 3o), which reads on forming a first structural layer over the first sacrificial layer

removing sacrificial layer 40/first sacrificial layer and layer 24/second sacrificial layer by etching using a selective etchant, the etching only removes a central portion (portions of layer 24 that interfaces with layers 48, 50/strips) of the sacrificial layer 24 without etching portion of layer 24 that is not contacted with the layers 48, 50/strips (col 11, lines 24-35), which reads on removing the first and second sacrificial layers by etching, the etching step etches the second layer at a greater rate within each portion of the second sacrificial which interfaces with any potion of the first strip in comparison to portion of the second sacrificial layer which are free from contact with the plurality of strips.

Regarding claim 40, fig. 4c shows that second sacrificial layer 24 is formed on layers 48, 50/strips. Regarding claim 41, fig. 4c also shows that layers 48, 50/strips remain after the step of removing the sacrificial layers. Regarding claims 48, 49, the layers 48, 50/strips are shown disposed parallel relation (fig. 4c). Regarding claims 50-56, Barron discloses forming the layers 48, 50/strips extending to a common center (fig. 4c), the layers 48, 50/strips are shown terminate at the same location (fig. 3q). Regarding claim 57, Barron discloses patterning layer 42/intermediate layer (fig. 3o)

4. Claims 58-59 are rejected under 35 U.S.C. 102(b) as being anticipated by Barron et al (US 5,919,548)

Barron discloses a method for CMP of recessed microelectromechanical devices. This method comprises the steps of:

forming a first sacrificial layer 40 over a first substrate 10, (col 10, lines 6-7, fig. 31), forming a plurality of laterally extending regions 48 and 54 that are positioned alongside the sidewall of etch channels 52 within the layer 40 (fig.4c), which reads on forming a plurality of at least generally laterally extending low density regions within the first sacrificial layer since "low density regions" are defined as regions alongside of etch release conduit in the sacrificial layer in page 88 of the specification

forming a layer 44 (polysilicon) over layer 40/first sacrificial layer (col 10, lines 48-49; fig. 3o), which reads on forming a first structural layer over the first sacrificial layer

removing sacrificial layer 40/first sacrificial layer by etching using a selective etchant, the etching only removes a central portion of layer 40 near the etch channels

52 (col 11, lines 31-35, fig. 3r shows that the etch removes regions of layer 40 alongside etch channels 50 without removing the regions 46), which reads on etching the first sacrificial layer at a greater rate within each of the plurality of low density regions than outside the plurality of low density regions.

Regarding claim 59, Barron discloses the step of forming layer 16/intermediate layer over the substrate, the layer 16 is disposed between the layer 40/first sacrificial layer and the first substrate 10 (fig.3q), patterning layer 16/intermediate layer into laterally extending layers/strips (fig. 3r)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barron et al (US 5,919,548) in view of Koyama (US 5,604,382)

Barron's method has been described above in paragraph 2. Unlike the instant claimed invention as per claim 16, Barron fails to disclose the specific thickness of the first subassembly (SiN).

However, Koyama, in a method of forming a semiconductor device, teaches that the thickness of the SiN is variable or controllable (col 8, lines 14-15)

Hence, one skilled in the art would have found it obvious to modify Barron by discovering the optimum value for the SiN thickness because Koyama discloses that the thickness is a result effective variable in the same field of endeavor.

7. Claims 63-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barron et al (US 5,919,548) in view of Fleming (US 5,867,302)

Barron discloses a method for CMP of recessed microelectromechanical devices. This method comprises the steps of:

forming a first sacrificial layer 40 over a first substrate 10, (col 10, lines 6-7, fig. 31)

forming a layer 44 (polysilicon) over layer 40/first sacrificial layer (col 10, lines 48-49; fig. 3o), which reads on forming a first structural layer over the first sacrificial layer

removing sacrificial layer 40/first sacrificial layer by etching, the etching step comprises using an etchant/first etchant to define the etch channel within the layer 40 and flowing another selective etchant/second etchant through etch channels 52 to remove layer 40/first sacrificial layer (col 11, lines 8-35)

Unlike the instant claimed invention as per claim 63, Barron fails to specifically disclose using a second etchant that is different from the first etchant to remove the first sacrificial layer.

However, Fleming discloses a method for forming microelectromechanical device comprises the step of using a second etchant HF that is different from the first etchant (XeF_2) to remove the first sacrificial layer (col 5, lines 9-19)

Since both Barron and Fleming are concerned with method of forming microelectromechanical device, one skilled in the art would have found it obvious to modify Barron method by using a second etchant that is different from the first etchant to remove the first sacrificial layer as per Fleming because Fleming states that his etchant composition is selected to dissolve the sacrificial layer but not to substantially attack any other material that surround the sacrificial layer thereby allowing the other material to act as an etch stop (col 6, lines 38-44)

Regarding claim 64, Barron discloses using a selective etchant to dissolve the sacrificial layer without affecting other material (col 11, lines 23-25)

Regarding claim 65, Barron discloses encasing etch channels/hollow conduits with etch release rails 48 (fig. 4b)

Regarding claim 66, Barron discloses forming a stack comprises layer 40/first sacrificial layer, layer 44/first structural layer, substrate 10 and exterior surface 54 opposite substrate 10, forming runner 54 that is laterally spaced from the layer 44/first structural layer, layer 54/runner also interconnects with rails 48 (fig. 4c).

Allowable Subject Matter

8. Claims 21, 42-47, 60-62 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 21, the cited prior art of record fails to disclose the step of forming a first sacrificial layer over the first intermediate layer wherein forming the sacrificial layer fails to fill an entirety of the spacing between the adjacent pairs of the plurality of strips. The closest prior art of Barron (US 5,919,548) discloses forming the first sacrificial layer 40 filling an entirety of the spacing between the adjacent pairs of the plurality of strips 48, 50 (fig. 3q)

Regarding claim 42, the cited prior art of record fails to disclose the step of forming a first structural layer after the step of etching through the second sacrificial layer to expose the plurality of first strips. In the contrary, the closest prior art of Barron (US 5,919,548) discloses the step of forming a first structural layer 42 prior to the step of etching through the second sacrificial layer to expose the plurality of first strips.

Regarding claim 60, the cited prior art of record fails to disclose the step of patterning the second sacrificial layer to define a plurality of at least generally laterally extending apertures, wherein each aperture comprises first and second aperture sidewalls that are disposed in spaced relation. Since the closest prior art of Barron (US 5,919,548) discloses forming a second sacrificial layer 24 to cover functional element 20, it would not have been obvious to form aperture in the sacrificial layer 24 to expose element 20.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
June 23, 2003